WE CLAIM:

1. A memory for storing data comprising:

a fast data reading mechanism operable to read a data value from said memory to generate a fast read result that is output from said memory for further processing;

a slow data reading mechanism operable to read said data value from said memory to generate a slow read result available after said fast read result has been output for further processing, said slow data reading mechanism being less prone to error in reading said data value than said fast data reading mechanism;

a comparator operable to compare said fast read result and said slow read result to detect if said fast read result differs from said slow read result; and

error repair logic operable if said comparator detects that said fast read result differs from said slow read result to suppress said further processing using said fast read result, to output said slow read result in place of said fast read result and to restart said further processing based upon said slow read result.

2. A memory as claimed in claim 1, comprising an array of memory cells, a data value stored in a memory cell within said array of memory cells being read via one or more bit lines.

3. A memory as claimed in claim 2, wherein said fast data reading mechanism is operable to sample said one or more bit lines at a time a first delay interval following said memory cell being coupled to said one or more bit lines and slow data reading mechanism is operable to sample said one or more bit lines at a time a second delay interval following said memory cell being coupled to said one or more bit lines, said second delay interval being greater than said first delay interval.

4. A memory as claimed in claim 2, wherein said memory cell is read via a pair of bit lines.

5. A memory as claimed in claim 4, wherein one or more differential sense amplifiers are operable to read signal values from said pair of bit lines.

6. A memory as claimed in claim 1, wherein said fast read mechanism and said slow read mechanism share at least some common circuit elements.

7. A memory as claimed in claim 1, wherein said error-repair logic is operable to suppress said further processing by issuing a suppression signal to circuits to which said fast read result has been passed for further processing.

8. A memory as claimed in claim 1, wherein one or more performance controlling parameters of said memory are controlled to maintain a non-zero error rate in said fast read result.

9. A memory as claimed in claim 8, wherein said one or more performance controlling parameters include one or more of:

operating voltage;

operating frequency;

body bias voltage; and

temperature.

10. A method of reading stored data from a memory, said method comprising the steps of:

reading a data value with a fast data reading mechanism from said memory to generate a fast read result that is output from said memory for further processing;

reading said data value with a slow data reading mechanism from said memory to generate a slow read result available after said fast read result has been output for further processing, said slow data reading mechanism being less prone to error in reading said data value than said fast data reading mechanism;

comparing said fast read result and said slow read result to detect if said fast read result differs from said slow read result; and

if said fast read result differs from said slow read result, then suppressing said further processing using said fast read result, outputting said slow read result in place of said fast read result and restarting said further processing based upon said slow read result.

11. A method as claimed in claim 10, wherein said memory comprise an array of memory cells, a data value stored in a memory cell within said array of memory cells being réad via one or more bit lines.

12. A method as claimed in claim 11, wherein said fast data reading mechanism is operable to sample said one or more bit lines at a time a first delay interval following said memory cell being coupled to said one or more bit lines and slow data reading mechanism is operable to sample said one or more bit lines at a time a second delay interval following said memory cell being coupled to said one or more bit lines, said second delay interval being greater than said first delay interval.

13. A method as claimed in claim 11, wherein said memory cell is read via a pair of bit lines.

14. A method as claimed in claim 13, wherein one or more differential sense amplifiers are operable to read signal values from said pair of bit lines.

15. A method as claimed in claim 10, wherein said fast read mechanism and said slow read mechanism share at least some common circuit elements.

16. A method as claimed in claim 10, wherein said error-repair logic is operable to suppress said further processing by issuing a suppression signal to circuits to which said fast read result has been passed for further processing.

17. A method as claimed in claim 10, wherein one or more performance controlling parameters of said memory are controlled to maintain a non-zero error rate in said fast read result.

18. A method as claimed in claim 17, wherein said one or more performance controlling parameters include one or more of:

operating voltage;
operating frequency;
body bias voltage; and
temperature